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REMARKS

In response to the above identified Office Action, Applicant respectfully requests reconsideration in view of the following remarks. Applicant has not added, amended or cancelled any claims. Accordingly, claims 1-16 are pending.

I. Objections to the Drawings

The Examiner has objected to Figure 1 and requested that it be designated as prior art. The Examiner states that "only that which is old is illustrated". Applicant respectfully disagrees. Figure 1 includes the element of a system memory labeled with reference number 113. This component and its subcomponents include elements which Applicant believes are novel and non-obvious. This same component is illustrated in Figures 2 and 3. Figure 3 clearly shows that this component encompasses elements such as the descriptor list table 303 and data buffer 307, which Applicant believes are novel and non obvious elements. Therefore, reconsideration and withdrawal of the objection to Figure 1 are requested.

II. Claims Rejected Under 35 U.S.C. § 101

Claims 14-16 stand rejected under 35 U.S.C. § 101 as allegedly directed to non statutory subject matter. The Examiner has rejected these claims because the "machine readable medium" element recited in these claims allegedly does not meet the "useful, concrete, and tangible" requirements set forth in *State Street*. However, the Examiner has improperly applied the test set forth in *State Street*. The "useful, concrete, and tangible" test of *State Street* is a test of the results of the claimed invention not a test of the component elements of the claimed invention. Thus, the Examiner misunderstood and misapplied *State Street* in holding that these claims are

directed toward non-statutory subject matter. See *State Street*, 47 USPQ.2d at 1602 ("For purposes of our analysis, as noted above, claim 1 is directed to a machine programmed with the hub and spoke software and admittedly produces a 'useful, concrete, and tangible *result*.' *Allapat*, 33 F.3d at 1544, 31 USPQ.2d at 1557. This renders it statutory subject matter even if the useful result is expressed in numbers, such as price, profit, percentage, costs or loss." (emphasis added)). Therefore, Applicant respectfully requests reconsideration and review of the non- statutory subject matter rejection of claims 14-16.

III. Claims Rejected Under 35 U.S.C. § 112

Claim 7 has been rejected under 35 U.S.C. § 112, first paragraph as allegedly, failing to comply with the written description requirement.

The Examiner alleges that the specification does not disclose "a memory device is a register in a memory controller" or how it is implemented in claim 7. However, paragraph [0018] specifically states "DMA controller 217, audio controller 223, or similar device may store the base address of descriptor table 303 in a base address storage register 301" (emphasis added). It is well known to one of ordinary skill in the art that a register is a memory storage device. Thus, one of ordinary skill in the art would understand that this section of the specification teaches a base address storage register that may be part of a DMA controller. See also Figure 3. Thus, the Applicant believes that the requirements of 35 U.S.C. § 112, first paragraph, have been met. Accordingly, reconsideration and withdrawal of the written description rejection of claim 7 are requested.

IV. Claims Rejected Under 35 U.S.C. § 102

Claims 1-7 and 11-16 stand rejected under 35 U.S.C. § 102 as being allegedly anticipated by U.S. publication no. 2004/0148480 by Watt, et al (hereinafter "Watt"). Applicant respectfully disagrees for the following reasons.

To establish anticipation, the Examiner must show that the cited reference teaches each element of the claim. In regard to claim 1, this claim includes the elements of "preventing a read of the pointer." The Examiner cites paragraph [0453] and page 25, lines 24-32 as teaching these elements of claim 1. However, the cited section of Watt does not disclose preventing a read of a pointer. Rather, this section of Watt discloses preventing access to a secure memory region when a descriptor from a page table has been tampered with. Thus, the Examiner has not demonstrated that the cited reference teaches each of the elements of this claim.

Further, the Examiner has failed to read the claim as a whole and establish that the cited reference teaches the elements of the claim in the manner in which they are arranged. See *In re Bond*, USPQ.2d 1566 (Fed.Cir 1990). The Examiner has made a piecemeal rejection of the claims relying on disparate portions of the cited reference. Specifically, the Examiner has cited one aspect of the disclosure as teaching "writing a pointer relating to a location of data to a known location" but has relied on an unrelated section for disclosing "preventing a read of the pointer from the known location." Thus, the Examiner has failed to properly establish anticipation of claim 1. Accordingly, reconsideration and withdrawal of the anticipation of claim 1 are requested.

In regard to claims 2-7, these claims depend from independent claim 1, and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to independent

claim 1, these claims are not anticipated by Watt. Accordingly, reconsideration and withdrawal of the anticipation rejection of claims 2-7 are requested.

In regard to claim 11, this claim includes the elements of "means for determining a protected status of data." The Examiner has cited Figure 55 and page 13, paragraph [0279] as teaching these elements of claim 11. Applicant has reviewed the cited section of Watt and has been unable to discern any part therein that teaches these elements of Watt. Rather, these sections describe how a processor core may be operating in a secure or non-secure status. See paragraph [0279] "one major feature of the carbon core is the presence of the S bit, which indicates whether the core is in a secure (S=1) or non-secure (S=0) state." Thus, the Examiner has failed to establish that the cited reference teaches this element of claim 11. Further, the Examiner fails again to read the claim as a whole and cites disparate elements of unrelated sections of the cited reference. It is unclear how each of these sections operate on the same data as recited in each of the elements of claim 11. Therefore, the Examiner has failed to establish the anticipation of claim 11. Accordingly, reconsideration and withdrawal of the anticipation rejection of this claim are requested.

Claims 12 and 13 depend from independent claim 11 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to independent claim 11, these claims are not anticipated by Watt. Accordingly, reconsideration and withdrawal of the anticipation rejection of claims 12 and 13 are requested.

In regard to claim 14, this claims includes the elements of "determining the descriptor table base address register is set in a protected mode." The Examiner cites figure 55 and page 13, paragraph [0279] as teaching these elements of claim 14. However, it is unclear how these sections of Watt relate to this element of claim 14. As discussed above paragraph [0279] relates

to the tracking of the status of a processor core which is not equivalent to a determination of a protected mode for a descriptor base address register as set forth in claim 14. Thus, the Examiner has failed to establish that Watt teaches each of the elements of claim 14. Accordingly, reconsideration and withdrawal of the anticipation rejection of claim 14 are requested.

In regard to claims 15 and 16, these claims depend from claim 14 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to independent claim 14, these claims are not anticipated by Watt. Accordingly, reconsideration and withdrawal of the anticipation rejection of these claims are requested.

V. Claims Rejected Under 35 U.S.C. § 103

Claims 8-10 stand rejected under 35 U.S.C. § 103 as being allegedly being unpatenable over Watt in view of U.S. Publication No. 2004/0044906 by England et al. (hereinafter "England") in view of what the Examiner labels as Applicant admitted prior art (hereinafter "AAPA"). The Applicant respectfully disagrees for the following reasons.

To establish a *prima facie* case of obviousness, the Examiner must show that the cited references teach or suggest each of the elements of a claim. In regard to claim 8, this claim includes the elements of "a memory controller coupled to the memory device and processor, the memory controller to store a pointer to a descriptor list table and to prevent a read of the pointer when the pointer is in a protected mode." The Examiner relies on Watt for teaching these elements of claim 8. However, the cited section of Watt does not teach a memory controller having a point to a descriptor table. Rather, the sections of Watt disclose a processor that includes a secure translation table base address. Thus, the Examiner has failed to establish how Watt teaches or suggests this element of claim 8. The Examiner has not relied on and the

Applicant has been unable to discern that any part of England or the AAPA that teaches or suggests this element of claim 8. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for claim 8. Accordingly, reconsideration and withdrawal of the obviousness rejection of claim 8 are requested.

Claims 9 and 10 depend from independent claim 8 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to independent claim 8, these claims are not obvious over the cited references. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

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CONCLUSION

In view of the foregoing, it is believed that all claims now pending, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/5, 2006

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Melissa Stead 4-5-06

Melissa Stead *Date*